


EXHIBIT 010


U.S. Patent No. 7,769,893 (Goossens)*“Integrated circuit and method for establishing transactions”*

'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
<p>4. A method for exchanging messages in an integrated circuit comprising a plurality of modules, the messages between the plurality of modules being exchanged via a network</p>	<p>Without conceding that the preamble of claim 4 of the '9893 Patent is limiting, the Samsung Galaxy Z Flip 4 (hereinafter, the “Samsung product”) performs a method for exchanging messages in an integrated circuit comprising a plurality of modules, the messages between the plurality of modules being exchanged via a network, either literally or under the doctrine of equivalents.</p> <p>The Samsung product includes an integrated circuit. For example, the Samsung product includes the Qualcomm Snapdragon 8+ Gen 1 Mobile Platform system on chip (hereinafter, the “Snapdragon SoC”).</p> <div data-bbox="516 678 926 1153">  </div> <p>Samsung Galaxy Z Flip4</p> <p>Powered by Snapdragon 8+ Gen 1 Mobile Platform</p> <p>Get the phone that claps back. The Snapdragon 8+ Gen 1 powered Galaxy Z Flip4 from Samsung Mobile has launched in style. This sleek, pocket-sized smartphone allows you to snap hands-free photos with Flex Cam, makes checking notifications a breeze with its cover screen, and comes in a wide array of colors. Plus, take selfies with the Rear Camera while the Cover Screen gives you a real-time preview. Check yourself from afar with a full-screen view finder, or tap to see the original ratio to make sure everyone is in frame.</p> <p>https://www.qualcomm.com/snapdragon/device-finder/samsung-galaxy-z-flip4</p>

¹ The Samsung product is charted as a representative product made used, sold, offered for sale, and/or imported by Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

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	<p>The Snapdragon SoC comprises a plurality of modules, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU):</p> <div data-bbox="514 410 945 553">  <p>Snapdragon 8+ mobile platform Gen 1</p> </div> <div data-bbox="1562 435 1866 457">SPECIFICATIONS & FEATURES</div> <div data-bbox="514 626 741 651"> Artificial Intelligence <hr/> <p>Qualcomm® Adreno™ GPU</p> <hr/> <p>Qualcomm® Kryo™ CPU</p> <hr/> <p>Qualcomm® Hexagon™ Processor</p> <ul style="list-style-type: none"> • Fused AI Accelerator • Hexagon Tensor Accelerator • Hexagon Vector eXtensions • Hexagon Scalar Accelerator • Support for mix precision(INT8+INT16) • Support for all precisions (INT8, INT16, FP16) <hr/> <p>Qualcomm® Sensing Hub</p> <hr/> <p>5G Modem-RF System</p> <hr/> <p>Snapdragon® X65 5G Modem-RF System</p> <ul style="list-style-type: none"> • 5G mmWave and sub-6 GHz, standalone • (SA) and non-standalone (NSA) modes, FDD, TDD • Dynamic Spectrum Sharing • mmWave: 8 carriers, 2x2 MIMO • Sub-6 GHz: 4x4 MIMO • Qualcomm® 5G PowerSave 2.0 • Qualcomm® Smart Transmit™ 2.0 technology • Qualcomm® Wideband Envelope Tracking • Qualcomm® AI-Enhanced Signal Boost • Global 5G multi-SIM <hr/> <p>Downlink: Up to 10 Gbps</p> <hr/> <p>Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, CDMA 1x, EV-DO, GSM/EDGE</p> <hr/> <p>Camera</p> <hr/> <p>Qualcomm Spectra™ Image Signal Processor</p> <ul style="list-style-type: none"> • Triple 18-bit ISPs • Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP) • Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag • Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag • Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag • Up to 200 Megapixel Photo Capture <hr/> <p>Rec. 2020 color gamut photo and video capture</p> <hr/> <p>Up to 10-bit color depth photo and video capture</p> <hr/> <p>8K HDR Video Capture + 64 MP Photo Capture</p> <hr/> <p>10-bit HEIF: HEIC photo capture, HEVC video capture</p> <hr/> <p>Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision</p> <hr/> <p>8K HDR Video Capture @ 30 FPS</p> <hr/> <p>4K Video Capture @ 120 FPS</p> <hr/> <p>Slow-mo video capture at 720p @ 960 FPS</p> <hr/> <p>Bokeh Engine for Video Capture</p> <hr/> <p>Video super resolution</p> <hr/> <p>Multi-frame Noise Reduction (MFNR)</p> <hr/> <p>Locally Motion Compensated Temporal Filtering</p> <hr/> <p>Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support</p> <hr/> <p>AI-based face detection, auto-focus, and</p> <hr/> <p>CPU</p> <hr/> <p>Kryo CPU</p> <ul style="list-style-type: none"> • Up to 3.2 GHz, with Arm Cortex-X2 technology • 64-bit Architecture <hr/> <p>Visual Subsystem</p> <hr/> <p>Adreno GPU</p> <ul style="list-style-type: none"> • Vulkan® 1.1 API support • HDR gaming (10-bit color depth, Rec. 2020 color gamut) • Physically Based Rendering • Volumetric Rendering • Adreno Frame Motion Engine • API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1 • Hardware-accelerated H.265 and VP9 decoder • HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision <hr/> <p>Security</p> <hr/> <p>Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU)</p> <hr/> <p>Trust Management Engine</p> <hr/> <p>Qualcomm® wireless edge services (WES) and premium security features</p> <hr/> <p>Qualcomm® 3D Sonic Sensor and Qualcomm® 3D Sonic Max (fingerprint sensor)</p> <hr/> <p>Qualcomm® Type-1 Hypervisor</p> </div>


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	<div data-bbox="506 250 934 901"> <p>Wi-Fi & Bluetooth*</p> <hr/> <p>Qualcomm® FastConnect™ 6900 System</p> <ul style="list-style-type: none"> • Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), • Wi-Fi 5 (802.11ac), 802.11a/b/g/n • Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz, 6 GHz • Peak speed: 3.6 Gbps • Channel Bandwidth: 20/40/80/160 MHz • 8-stream sounding (for 8x8 MU-MIMO) • MIMO Configuration: 2x2 (2-stream) • MU-MIMO (Uplink & Downlink) • 4K QAM • OFDMA (Uplink & Downlink) • 4-Stream (2x2 + 2x2) Dual Band Simultaneous (DBS) • Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal <hr/> <p>Integrated Bluetooth</p> <ul style="list-style-type: none"> • Bluetooth Features: Bluetooth® 5.3, LE Audio, Dual Bluetooth antennas • Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm® aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio <hr/> <p>snapdragon.com</p> </div> <div data-bbox="976 250 1404 771"> <p>Audio</p> <hr/> <p>Qualcomm Aqstic™ audio codec (WCD9385)</p> <hr/> <p>New Qualcomm Aqstic smart speaker amplifier (WSA8835)</p> <hr/> <p>Total Harmonic Distortion + Noise (THD+N), Playback: -108dB</p> <hr/> <p>Qualcomm® Audio and Voice Communication Suite</p> <hr/> <p>Display</p> <hr/> <p>On-Device Display Support:</p> <ul style="list-style-type: none"> • 4K @ 60 Hz • QHD+ @ 144 Hz <hr/> <p>Maximum External Display Support: up to 4K @ 60 Hz</p> <ul style="list-style-type: none"> • 10-bit color depth, Rec. 2020 color gamut • HDR10 and HDR10+ <hr/> <p>Demura and subpixel rendering for OLED Uniformity</p> </div> <div data-bbox="1446 250 1875 868"> <p>Charging</p> <hr/> <p>Qualcomm® Quick Charge™ 5 Technology</p> <hr/> <p>Location</p> <hr/> <p>GPS, Glonass, BeiDou, Galileo, QZSS, NavIC capable</p> <hr/> <p>Dual Frequency GNSS (L1/L5)</p> <hr/> <p>Sensor-Assisted Positioning</p> <ul style="list-style-type: none"> • Urban pedestrian navigation with sidewalk accuracy • Global freeway lane-level vehicle navigation <hr/> <p>Memory</p> <hr/> <p>Support for LP-DDR5 memory up to 3200 MHz</p> <hr/> <p>Memory Density: up to 16 GB</p> <hr/> <p>General Specifications</p> <hr/> <p>Full Suite of Snapdragon Elite Gaming™ features</p> <hr/> <p>4 nm Process Technology</p> <hr/> <p>USB Version 3.1; USB Type-C Support</p> <hr/> <p>Part Number: SM8475</p> </div> <div data-bbox="506 954 1875 1084" style="background-color: #f0f0f0; padding: 10px; margin-top: 20px;"> <p><small>*Snapdragon 8+ Gen 1 Mobile Platform also available in 3 GHz CPU version. Maximum CPU speed will vary based on platform version. Consult OEM specifications for device CPU speed. Certain optional features available subject to Carrier and OEM selection for an additional fee.</small></p> <p><small>Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm 5G PowerSave, Qualcomm Kiyo, Qualcomm Smart Transmit, Qualcomm Wideband Envelope Tracking, Qualcomm AI Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Aqstic, Qualcomm 3D Sonic Sensor, Qualcomm Type-1 Hypervisor, Qualcomm Adreno, Qualcomm Sensing Hub, Qualcomm 3D Sonic Max, Qualcomm FastConnect, Snapdragon Sound, Qualcomm aptX, Snapdragon Elite Gaming, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries.</small></p> <p><small>Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kiyo, Smart Transmit, Qualcomm Spectra, Qualcomm Aqstic, Snapdragon Sight, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd. ©2022 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</small></p> </div> <div data-bbox="491 1128 1463 1209" data-label="Text"> <p>https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf</p> </div> <div data-bbox="491 1247 1766 1367" data-label="Text"> <p>The Snapdragon SoC included in the Samsung product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) for exchanging messages:</p> </div>

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	<div data-bbox="512 336 1066 1019"><p data-bbox="558 386 768 435">Qualcomm</p><p data-bbox="558 638 1003 813">Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products.</p><div data-bbox="663 885 909 958"><p data-bbox="701 911 871 932">LEARN MORE »</p></div></div> <p data-bbox="501 1073 1713 1105">https://web.archive.org/web/20210514110614/https://www.artemis.com/customers</p>

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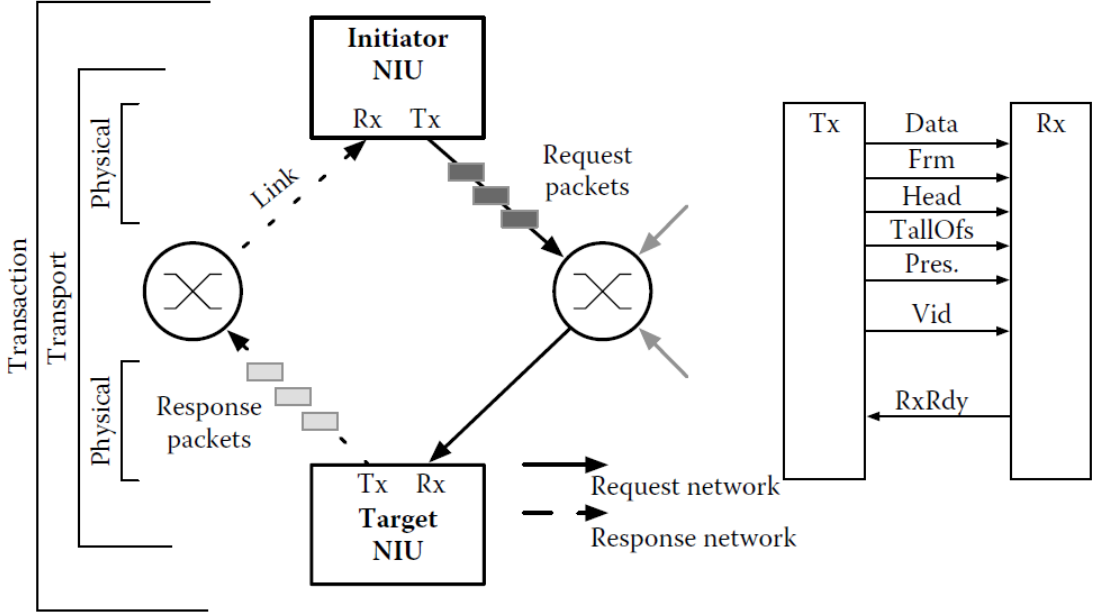
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	<p data-bbox="575 253 1360 302">Certain Arteris Technology Assets Acquired</p> <p data-bbox="785 331 1150 358">by Kurt Shuler, on October 31, 2013</p> <p data-bbox="512 396 1255 423">Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p data-bbox="512 448 1417 553">SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p data-bbox="512 586 1360 732">“Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology.</p> <p data-bbox="1234 773 1377 800">ARTERIS </p> <p data-bbox="1119 849 1377 867"><i>K. Charles Janac, President and CEO, Arteris</i></p> <p data-bbox="499 935 1797 1008">https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team</p> <p data-bbox="499 1049 1797 1130">The Arteris NoC exchanges messages between the plurality of modules via a network in the Snapdragon SoC included in the Samsung product.</p> <p data-bbox="499 1170 1843 1243">For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

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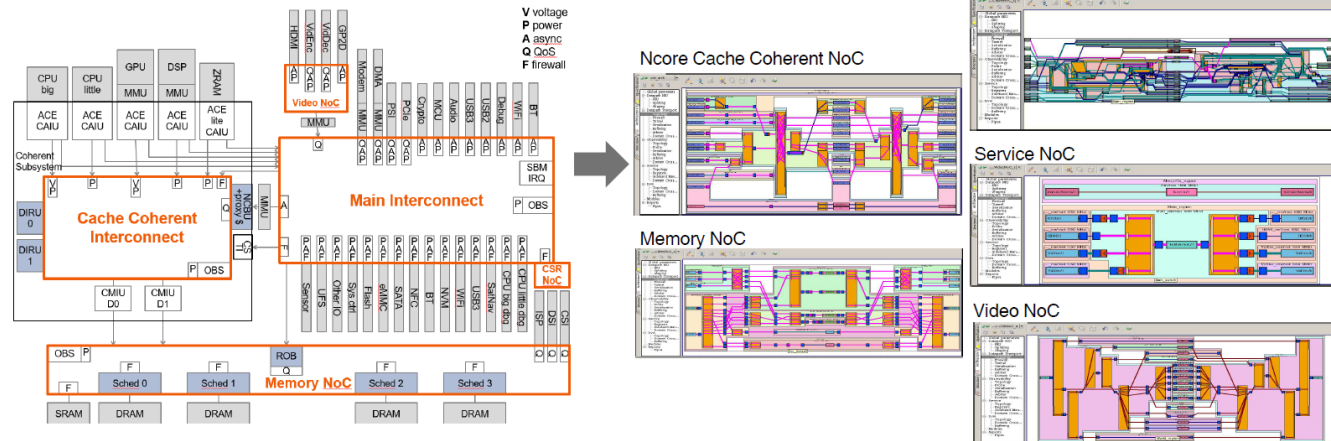

'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p> <p>As a further illustration, a large SoC, such as the Snapdragon SoC included in the Samsung product may include multiple classes of Arteris NoC network:</p>

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	<p style="text-align: center;">Logical Interconnect Topology Development</p> <p style="text-align: center;">FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p>  <ul style="list-style-type: none"> • ArChip16 Example: Large SoCs have multiple classes of interconnect <ul style="list-style-type: none"> – Non-coherent, Coherent, Control/Status, Observability, etc. • Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility <p style="text-align: center;">  ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 9 </p> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.</p>
wherein a message issued by an addressing module M in the Snapdragon SoC included in the Samsung product via the Arteris NoC comprises first information indicative of a location of an addressed message receiving module S within the network and is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface means associated with the addressed message receiving module S, and second information	

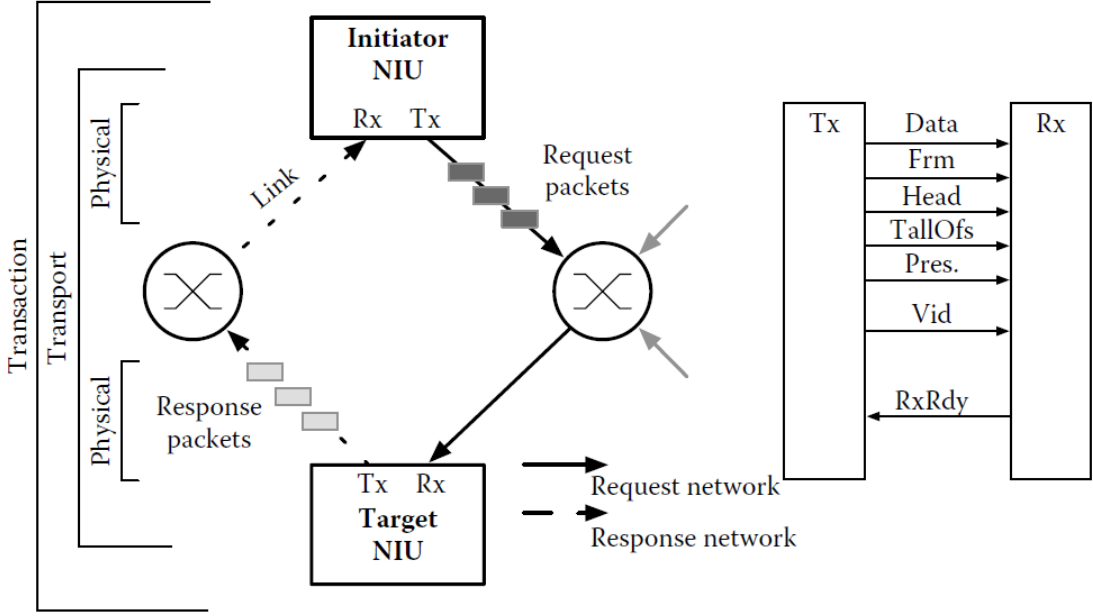
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<p>first information indicative of a location of an addressed message receiving module S within the network and is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface means associated with the addressed message receiving module S, and second information indicative of a particular location within the addressed message receiving module S, such as</p>	<p>indicative of a particular location within the addressed message receiving module S, such as a memory, or a register address, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC used in the Snapdragon SoC included in the Samsung product uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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a memory, or a register address,	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>As a further illustration, connections between initiator module NIUs (e.g., “CPUbigAIU/1/0”) and two or more target module NIUs (e.g., “ETTarg/T/0,” “EMMC/T/0,” “Flash/T/0,” “NFC/T0,” “PCIeTarg/T/0,” etc.) within the Arteris NoC may be defined by a connectivity table:</p>

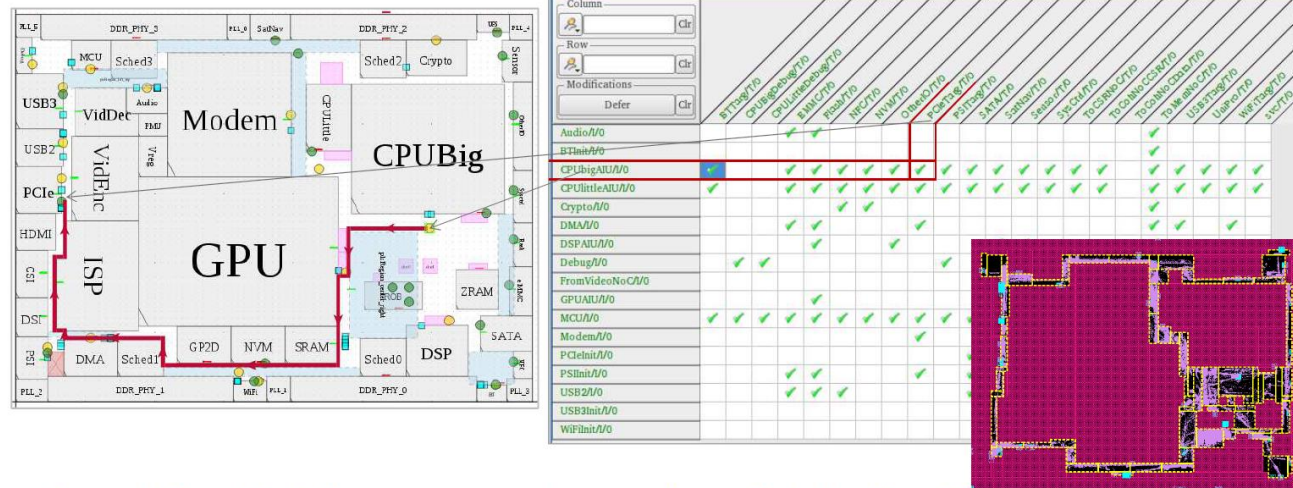
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Connectivity Map → Interconnect Connections → Layout



DC-Topographical

- Connectivity table defines interconnect connections within the floorplan
- Routes must pass through available channels in the floorplan
- Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU

ARTERIS IP

ISPD 2018, 28 March 2018

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.

As a further illustration, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”:

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	<p data-bbox="514 267 919 305">11.3.1.2 Transport Layer</p> <p data-bbox="514 321 1709 743">The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p data-bbox="504 764 1854 841"><i>See</i> Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313.</p> <p data-bbox="504 883 1829 995">As a further example, the packets sent in the Arteris NoC are “composed of cells that are organized into fields, with each field carrying specific information,” including “Slave address” and “Slave offset”:</p>

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	Field	Size	Function
	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
	MstAddr	User Defined	Master address
	SlvAddr	User Defined	Slave address
	SlvOfs	User Defined	Slave offset
	Len	User Defined	Payload length
	Tag	User Defined	Tag
	Prs	User defined (0 to 2)	Pressure
	BE	0 or 4 bits	Byte enables
	CE	1 bit	Cell error
	Data	32 bits	Packet payload
	Info	User Defined	Information about services supported by the NoC
	Err	1 bit	Error bit
	StartOfs	2 bits	Start offset
	StopOfs	2 bits	Stop offset
	WrpSize	4 bits	Wrap size
	Rsv	Variable	Reserved
	CtlId	4 bits/3 bits	Control identifier, for control packets only
	CtlInfo	Variable	Control information, for control packets only
	EvtId	User defined	Event identifier, for event packets only

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	<p>FIGURE 11.2 NTTP packet structure.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.</p> <p>As a further example, “[i]nitiator NIU units...translate[] AHB transactions AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP” and the “AHB-to-NTTP unit instantiates a Translation Table for address decoding” with the table “receiv[ing] 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p> <p>As further example, “[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)”:</p>

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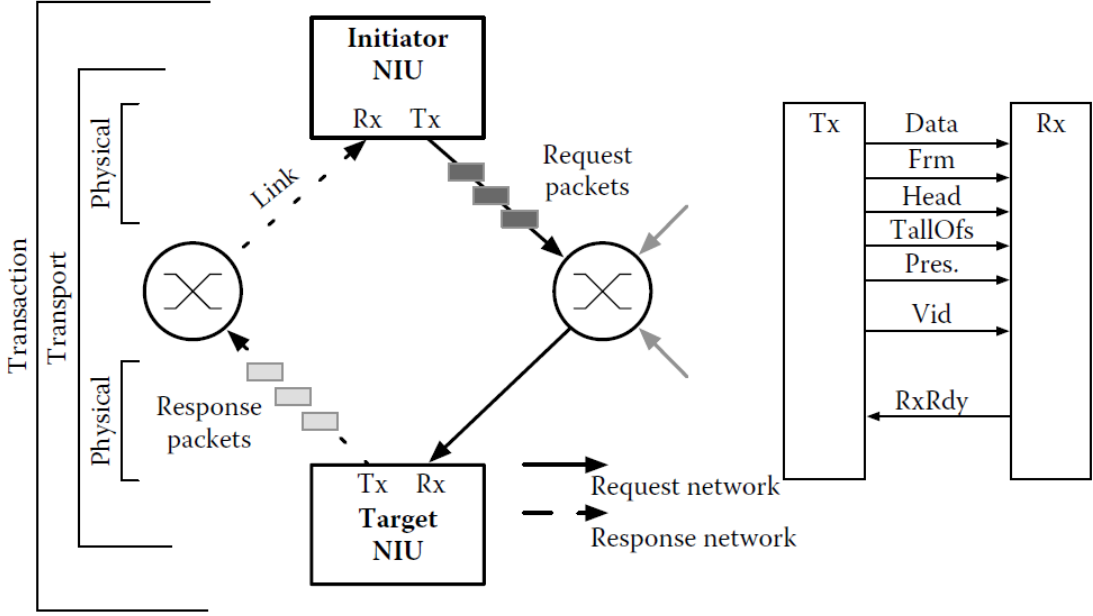
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	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always</p> <p><i>Id.</i> at 318.</p>
<p>the method including the steps of:</p> <p>(a) issuing from said addressing module M a message request including said first information, said second information, and data and/or connection properties to an address</p>	<p>The Arteris NoC utilized by the Snapdragon SoC included in the Samsung product issues from said addressing module M a message request including said first information, said second information, and data and/or connection properties to an address translation unit included as part of an active network interface module associated with said addressing module M, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC used in the Snapdragon SoC included in the Samsung product uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

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“Integrated circuit and method for establishing transactions”

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translation unit included as part of an active network interface module associated with said addressing module M,	<p data-bbox="558 266 1020 305">11.3.1.1 Transaction Layer</p> <p data-bbox="558 323 1822 500">The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul data-bbox="632 545 1350 639" style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p data-bbox="558 685 1822 816">As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p> <p data-bbox="548 846 1843 1255">on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>As a further illustration, connections between initiator module NIUs (e.g., “CPUbigAIU/1/0”) and two or more target module NIUs (e.g., “ETTarg/T/0,” “EMMC/T/0,” “Flash/T/0,” “NFC/T0,” “PCIeTarg/T/0,” etc.) within the Arteris NoC may be defined by a connectivity table:</p>

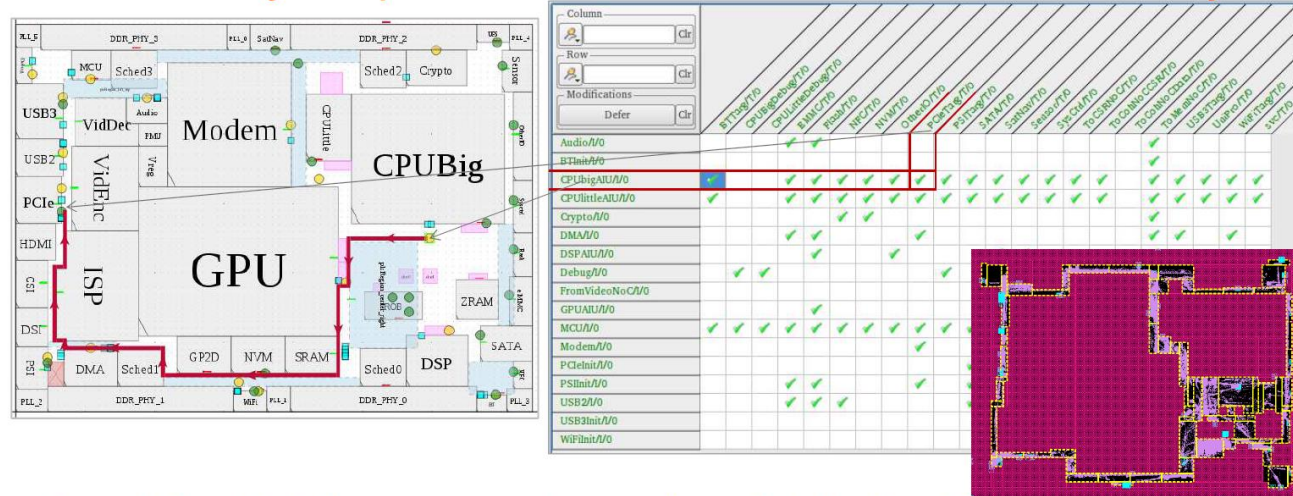
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"Integrated circuit and method for establishing transactions"

'9893 Patent Claim

Samsung Product Including Snapdragon System on Chip¹

Connectivity Map → Interconnect Connections → Layout



DC-Topographical

- Connectivity table defines interconnect connections within the floorplan
- Routes must pass through available channels in the floorplan
- Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.

As a further illustration, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”:

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	<p data-bbox="514 267 919 305">11.3.1.2 Transport Layer</p> <p data-bbox="514 321 1709 743">The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p data-bbox="514 764 632 797"><i>Id.</i> at 313.</p> <p data-bbox="514 846 1803 997">As yet a further illustration, packets in the Arteris NoC are “delivered as words that are sent along links and “[o]ne link (represented in Figure 11.1) defines the following signals,” which include “the current priority of the packet used to define preferred traffic class (or Quality of Service)” and “[f]low control”:</p>

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maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in [Figure 11.1](#)) defines the following signals:

- **Data**—Data word of the width specified at design-time.
- **Frm**—When asserted high, indicates that a packet is being transmitted.
- **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.
- **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.
- **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in [Figure 11.2](#)).
- **Vld**—Data valid: when asserted high, indicates that a word is being transmitted.
- **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy.

This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTPP communications.

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	<p><i>Id.</i> at 313-314.</p> <p>As a further example, the packets sent in the Arteris NoC are “composed of cells that are organized into fields, with each field carrying specific information,” including “Pres,” “Slave address” and “Slave offset”:</p> <table><tr><th>Field</th><th>Size</th><th>Function</th></tr><tr><td>Opcode</td><td>4 bits/3 bits</td><td>Packet type: 4 bits for requests, 3 bits for responses</td></tr><tr><td>MstAddr</td><td>User Defined</td><td>Master address</td></tr><tr><td>SlvAddr</td><td>User Defined</td><td>Slave address</td></tr><tr><td>SlvOfs</td><td>User Defined</td><td>Slave offset</td></tr><tr><td>Len</td><td>User Defined</td><td>Payload length</td></tr><tr><td>Tag</td><td>User Defined</td><td>Tag</td></tr><tr><td>Prs</td><td>User defined (0 to 2)</td><td>Pressure</td></tr><tr><td>BE</td><td>0 or 4 bits</td><td>Byte enables</td></tr><tr><td>CE</td><td>1 bit</td><td>Cell error</td></tr><tr><td>Data</td><td>32 bits</td><td>Packet payload</td></tr><tr><td>Info</td><td>User Defined</td><td>Information about services supported by the NoC</td></tr><tr><td>Err</td><td>1 bit</td><td>Error bit</td></tr></table>	Field	Size	Function	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses	MstAddr	User Defined	Master address	SlvAddr	User Defined	Slave address	SlvOfs	User Defined	Slave offset	Len	User Defined	Payload length	Tag	User Defined	Tag	Prs	User defined (0 to 2)	Pressure	BE	0 or 4 bits	Byte enables	CE	1 bit	Cell error	Data	32 bits	Packet payload	Info	User Defined	Information about services supported by the NoC	Err	1 bit	Error bit
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	StartOfs	2 bits	Start offset
	StopOfs	2 bits	Stop offset
	WrpSize	4 bits	Wrap size
	Rsv	Variable	Reserved
	CtlId	4 bits/3 bits	Control identifier, for control packets only
	CtlInfo	Variable	Control information, for control packets only
	EvtId	User defined	Event identifier, for event packets only

35

29 28

25 24

15 14

5 4 3

0

Header

Info

Len

Master Address

Slave Address

Prs

Opcode

Necker

Tag

Err

Slave offset

StartOfs

StopOfs

Data

BE

Data Byte

BE

Data Byte

BE

Data Byte

BE

Data Byte

Data

BE

Data Byte

BE

Data Byte

BE

Data Byte

BE

Data Byte

32 31 30

27 26

20 19

14 13

5 4 3

0

Header

Rsv

Len

Info

Tag

Master Address

Prs

Opcode

Data

CE

Data

Data

CE

Data

FIGURE 11.2

NTTP packet structure.

Networks-On-Chips Theory and Practice,

<https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>,

at 313, 314-315.

As a further example, “[i]nitiator NIU units...translate[] AHB transactions AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target

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'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p data-bbox="504 250 1869 402">NIU, that is, slave IP” and the “AHB-to-NTTP unit instantiates a Translation Table for address decoding” with the table “receiv[ing] 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size”:</p> <p data-bbox="504 461 1029 500">11.3.2.1 Initiator NIU Units</p> <p data-bbox="504 521 1837 1170">Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p data-bbox="504 1224 1806 1300">Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p>

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	<p>As further example, “[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)”:</p> <p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always</p> <p><i>Id.</i> at 318.</p> <p>As a further illustration, the Arteris NoC implements Quality of Service (QoS) to “provide[] a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic”; “QoS, which includes guarantees of throughput and/or latency, is achieved by exploiting the signal pressure embedded into the NTTP packet definition” where the “pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed”; and the “pressure information will be embedded in the NTTP packet at the NIU level”:</p>

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'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>Quality of Service (QoS). The QoS is a very important feature in the inter-connect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in <i>Æthereal NoC</i> [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT.</p> <p>In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure</p>

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'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair.</p> <p>The Arteris NoC supports the following four different traffic classes:</p>

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	<ul style="list-style-type: none"> • Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

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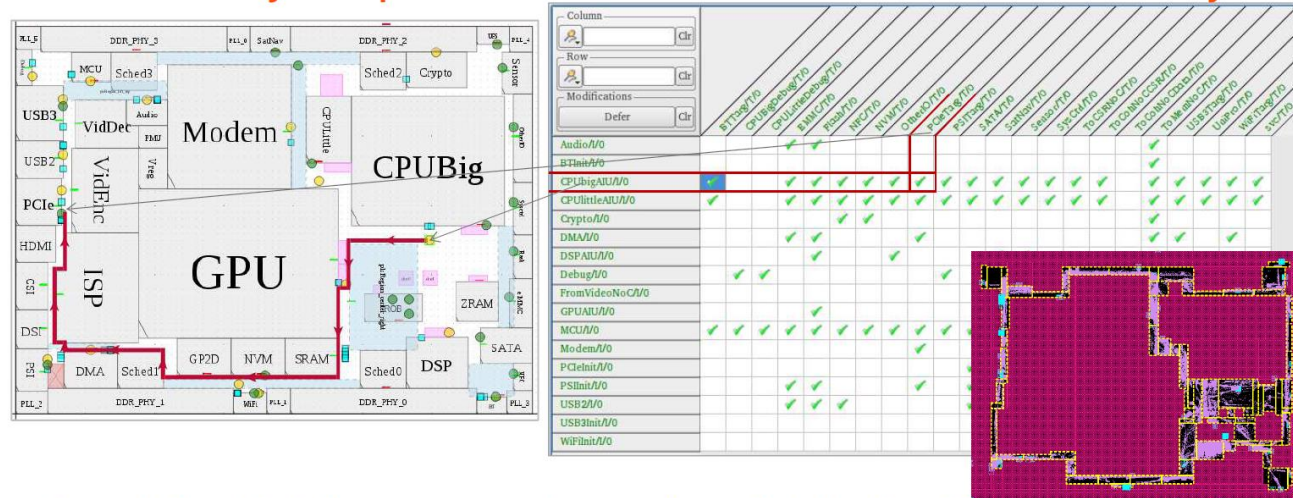
“Integrated circuit and method for establishing transactions”

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* Note that in the NTTP packet, the pressure field allows more than one bit, resulting in multiple levels of preferred traffic.

Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 315-316.

Connections within the Arteris NoC may be defined by a connectivity table:

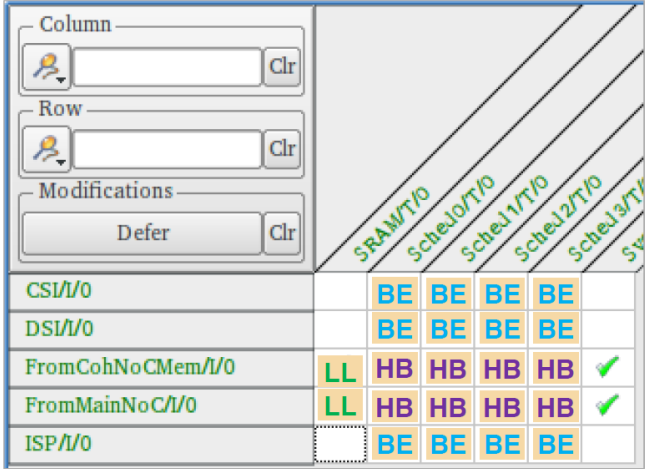
Connectivity Map → Interconnect Connections → Layout

- Connectivity table defines interconnect connections within the floorplan
- Routes must pass through available channels in the floorplan
- Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU

DC-Topographical

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“Integrated circuit and method for establishing transactions”

'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹						
	<p data-bbox="499 253 1879 326">See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.</p> <p data-bbox="499 370 1879 488">As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes, including related to latency, may be mapped onto the Arteris interconnect topology:</p> <p data-bbox="531 561 1465 659">Memory NoC: Interconnect Topology – Traffic Classes</p> <p data-bbox="531 719 1066 781">Classify your IP connections per class of traffic:</p> <table data-bbox="531 833 1119 963"> <tr> <td>Best Effort (BE)</td><td>Image system</td></tr> <tr> <td>Low Latency (LL)</td><td>SRAM</td></tr> <tr> <td>High Bandwidth (HB)</td><td>Main/Coherency</td></tr> </table>  <p data-bbox="506 1295 636 1320">ARTERISIP</p> <p data-bbox="1100 1300 1247 1317">ISPD 2018, 28 March 2018</p> <p data-bbox="1646 1300 1854 1317">Copyright © 2018 Arteris IP 13</p>	Best Effort (BE)	Image system	Low Latency (LL)	SRAM	High Bandwidth (HB)	Main/Coherency
Best Effort (BE)	Image system						
Low Latency (LL)	SRAM						
High Bandwidth (HB)	Main/Coherency						

U.S. Patent No. 7,769,893 (Goossens)

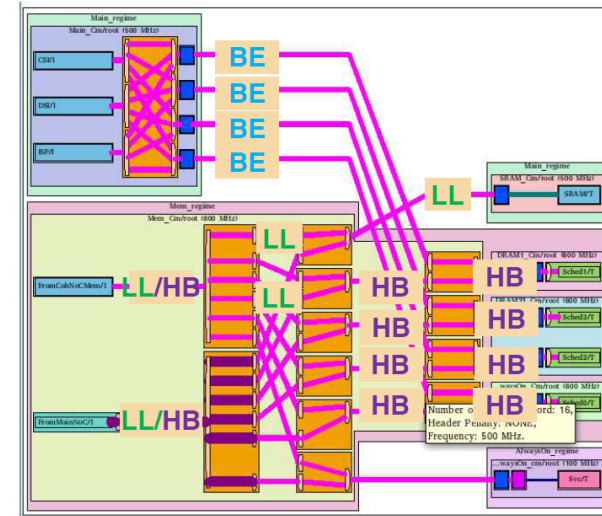
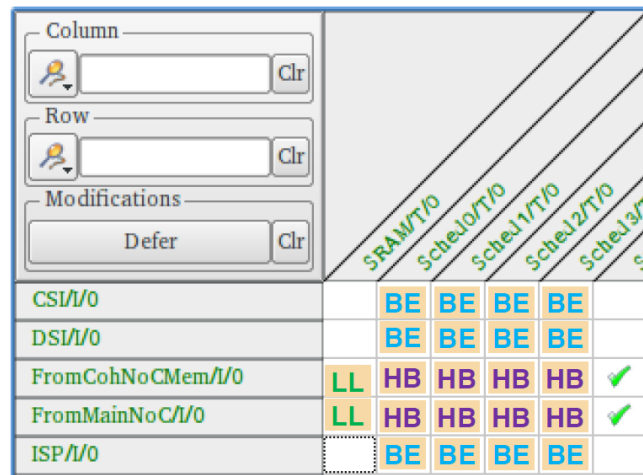
“Integrated circuit and method for establishing transactions”

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Memory NoC:

Traffic classes are mapped onto logical interconnect topology



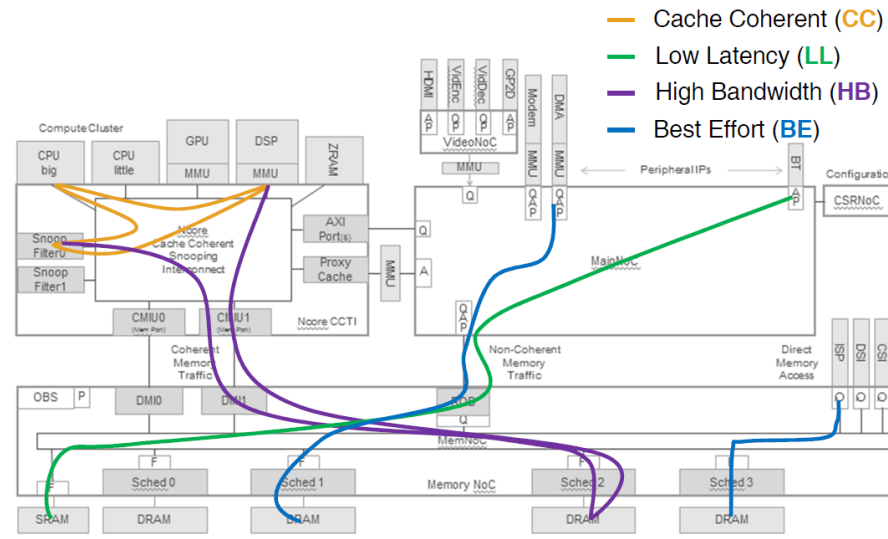
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	<h3 style="color: orange;">Memory Access Traffic Classes</h3>  <ul style="list-style-type: none"> — Cache Coherent (CC) — Low Latency (LL) — High Bandwidth (HB) — Best Effort (BE) <ul style="list-style-type: none"> • Cache Coherent (CC) within Compute Cluster • Low Latency (LL) to SRAM • High Bandwidth (HB) to DRAM & Cache Fill • Best Effort (BE) for Peripherals & DMA • QoS for Video • Multiple functional NoCs interacting • Physically Constrained <p style="font-size: small;"> ARTERISIP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 11 </p> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.</p>
(b) arranging, at said address translation unit, the first and the second	<p>The Arteris NoC utilized by the Snapdragon SoC included in the Samsung product arranges, at said address translation unit, the first and the second information comprising said issued message as a single address, either literally or under the doctrine of equivalents.</p>

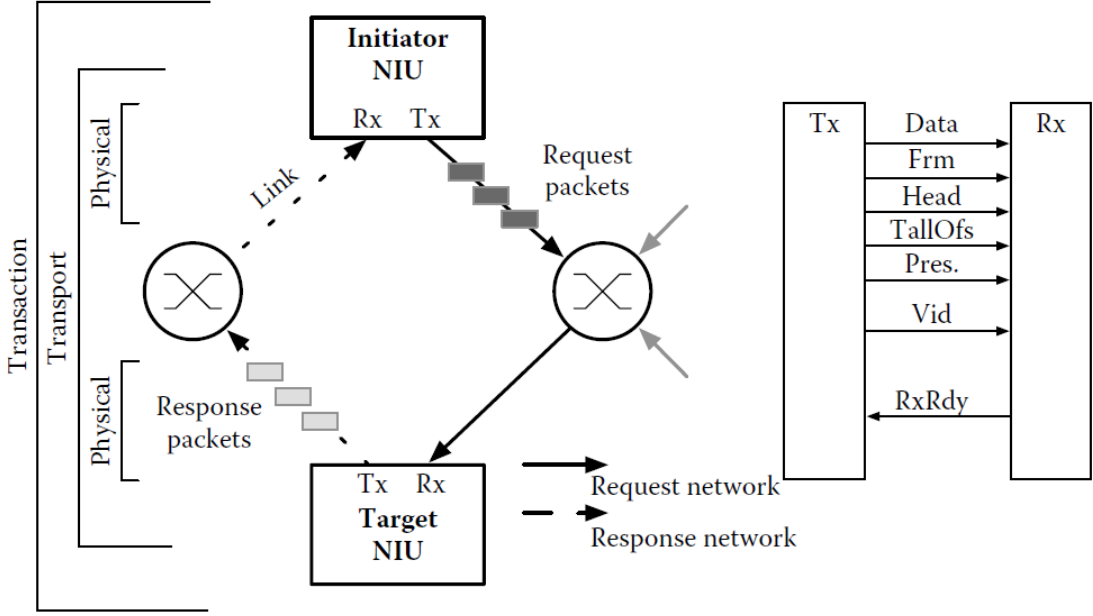
U.S. Patent No. 7,769,893 (Goossens)*“Integrated circuit and method for establishing transactions”*

'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
information comprising said issued message as a single address,	<p>For example, the Arteris NoC used in the Snapdragon SoC included in the Samsung product uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>As a further illustration, connections between initiator module NIUs (e.g., “CPUbigAIU/1/0”) and two or more target module NIUs (e.g., “ETTarg/T/0,” “EMMC/T/0,” “Flash/T/0,” “NFC/T0,” “PCIeTarg/T/0,” etc.) within the Arteris NoC may be defined by a connectivity table:</p>

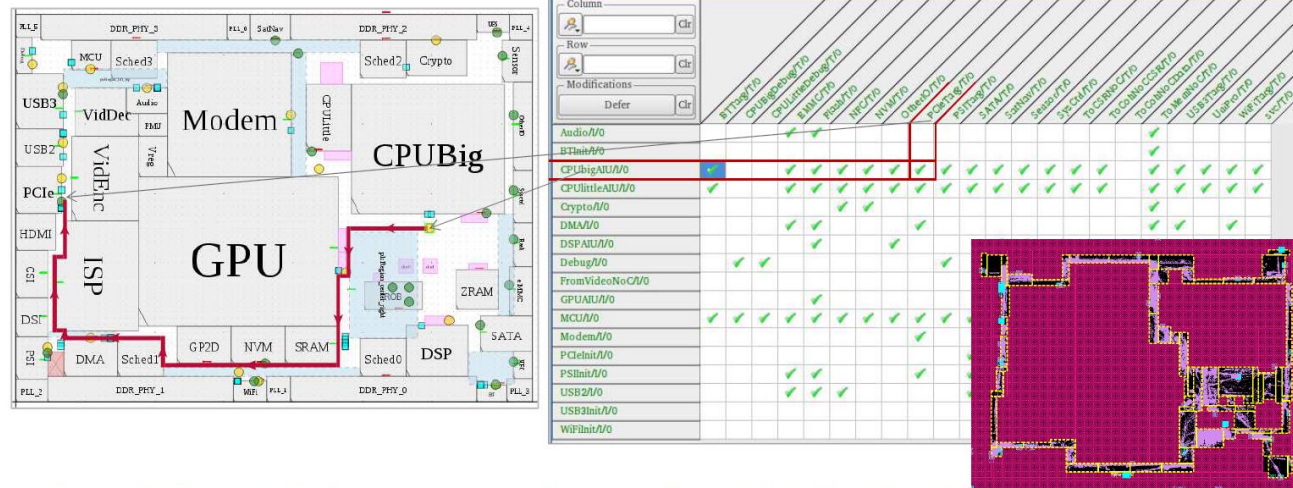
U.S. Patent No. 7,769,893 (Goossens)

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Connectivity Map → Interconnect Connections → Layout



DC-Topographical

- Connectivity table defines interconnect connections within the floorplan
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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.

As a further illustration, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”:

U.S. Patent No. 7,769,893 (Goossens)*“Integrated circuit and method for establishing transactions”*

'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p data-bbox="514 266 919 303">11.3.1.2 Transport Layer</p> <p data-bbox="514 321 1709 743">The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p data-bbox="514 764 632 797"><i>Id.</i> at 313.</p> <p data-bbox="514 846 1808 954">As a further example, the packets sent in the Arteris NoC are “composed of cells that are organized into fields, with each field carrying specific information,” including “Pres,” “Slave address” and “Slave offset”:</p>

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'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹		
	Field	Size	Function
	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
	MstAddr	User Defined	Master address
	SlvAddr	User Defined	Slave address
	SlvOfs	User Defined	Slave offset
	Len	User Defined	Payload length
	Tag	User Defined	Tag
	Prs	User defined (0 to 2)	Pressure
	BE	0 or 4 bits	Byte enables
	CE	1 bit	Cell error
	Data	32 bits	Packet payload
	Info	User Defined	Information about services supported by the NoC
	Err	1 bit	Error bit
	StartOfs	2 bits	Start offset
	StopOfs	2 bits	Stop offset
	WrpSize	4 bits	Wrap size
	Rsv	Variable	Reserved
	CtlId	4 bits/3 bits	Control identifier, for control packets only
	CtlInfo	Variable	Control information, for control packets only
	EvtId	User defined	Event identifier, for event packets only

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'9893 Patent Claim	Samsung Product Including Snapdragon System on Chip ¹
	<p>FIGURE 11.2 NTTP packet structure.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.</p> <p>As a further example, “[i]nitiator NIU units...translate[] AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP” and the “AHB-to-NTTP unit instantiates a Translation Table for address decoding” with the table “receiv[ing] 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p>
(c) determining, at said address translation unit, which message receiving module S is being addressed in said	<p>The Arteris NoC utilized by the Snapdragon SoC included in the Samsung product determines, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC used by the Snapdragon SoC included in the Samsung product uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB,</p>

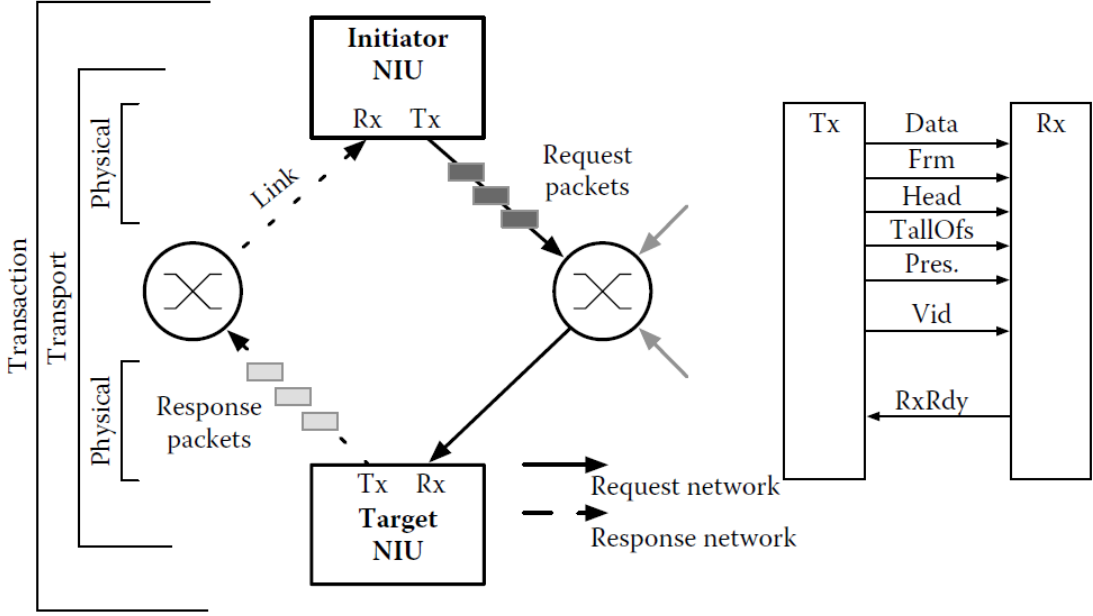
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message request issued from said addressing module M based on said single address, and	<p>and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.</p> <p>As a further illustration, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”:</p>

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	<p>11.3.1.2 Transport Layer</p> <p>The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p><i>Id.</i> at 313.</p> <p>As a further example, the packets sent in the Arteris NoC are “composed of cells that are organized into fields, with each field carrying specific information,” including “Slave address” and “Slave offset”:</p>

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	Field	Size	Function
	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
	MstAddr	User Defined	Master address
	SlvAddr	User Defined	Slave address
	SlvOfs	User Defined	Slave offset
	Len	User Defined	Payload length
	Tag	User Defined	Tag
	Prs	User defined (0 to 2)	Pressure
	BE	0 or 4 bits	Byte enables
	CE	1 bit	Cell error
	Data	32 bits	Packet payload
	Info	User Defined	Information about services supported by the NoC
	Err	1 bit	Error bit
	StartOfs	2 bits	Start offset
	StopOfs	2 bits	Stop offset
	WrpSize	4 bits	Wrap size
	Rsv	Variable	Reserved
	CtlId	4 bits/3 bits	Control identifier, for control packets only
	CtlInfo	Variable	Control information, for control packets only
	EvtId	User defined	Event identifier, for event packets only

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	<p>FIGURE 11.2 NTTP packet structure.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.</p> <p>As a further example, “[i]nitiator NIU units...translate[] AHB transactions AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP” and the “AHB-to-NTTP unit instantiates a Translation Table for address decoding” with the table “receiv[ing] 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size”:</p>

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	<p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p> <p>As further example, “[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)”:</p>

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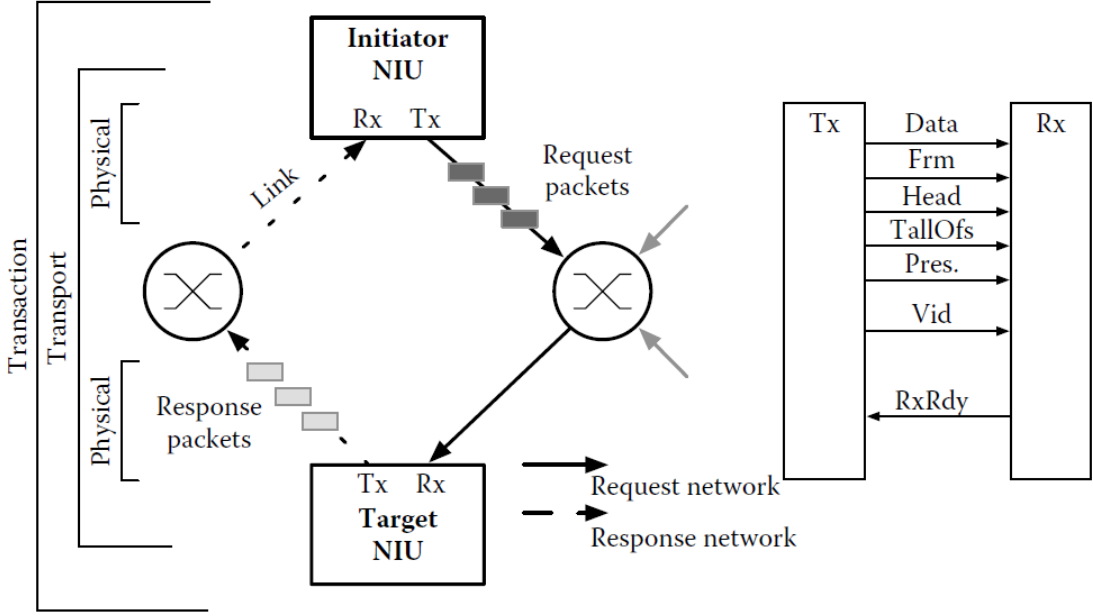
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	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always</p> <p><i>Id.</i> at 318.</p>
(d) further determining, at said address translation unit, the particular location within the addressed message receiving module S based on said single address.	<p>The Arteris NoC utilized by the Snapdragon SoC included in the Samsung product further determines, at said address translation unit, the particular location within the addressed message receiving module S based on said single address, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

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	<p data-bbox="562 267 1020 305">11.3.1.1 Transaction Layer</p> <p data-bbox="562 324 1822 500">The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul data-bbox="632 545 1350 641" style="list-style-type: none"> <li data-bbox="632 545 1199 586">• A master sends request packets. <li data-bbox="632 597 1350 641">• Then, the slave returns response packets. <p data-bbox="562 686 1822 816">As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p> <p data-bbox="548 886 1843 1295">on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	Prs	User defined (0 to 2)	Pressure
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	Err	1 bit	Error bit
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	CtlId	4 bits/3 bits	Control identifier, for control packets only
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